

# ELECTRONIC COUNTERS

## Modulation Domain Analyzer Applications

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The application examples on this page and the next illustrate some of the many situations that benefit from HP modulation domain analyzers. For complete product specifications or to arrange a product demonstration, contact the HP sales office in your area.

### Modulation Analysis for Mobile Communications

The HP 53310A's Option 031 "Digital RF Communications Analysis/High Resolution 2.5 GHz Input" provides automatic measurements of synthesizer settling time, Frequency Shift Keyed (FSK) center frequency, and FSK peak deviation on DECT, CT2, and CT3 radios. Features for optimizing RF designs include:

- High resolution measurements—built-in downconversion provides superior frequency resolution for RF signals.
- RF envelope trigger—simplifies measurement setup by automatically triggering on a detected TDMA burst.
- Automatic measurements—synthesizer settling time, Frequency Shift Keyed (FSK) center frequency, and FSK deviation.

### Data Storage Analysis

The HP E1725A Option 141 instrument is tailored for the specific requirements of data storage analysis. High-speed measurements and the large 512K on-board memory allow you to measure a full track on today's high data-rate drives. Complete acquisition control allows measuring data edges in the presence of servo or header fields. The Option 141 TIA software can be combined with the Option 147 timing pattern analysis software to provide powerful display and analysis capabilities:

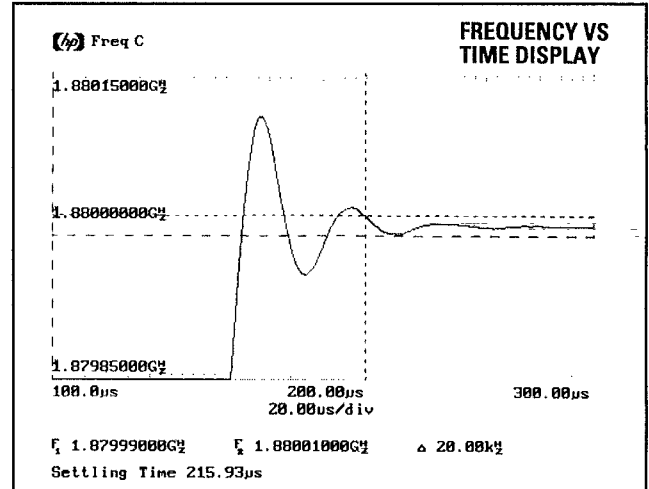
- Window margin analysis and histograms for understanding drive timing (view peak shift, jitter, worst-case data patterns)
- Flexible measurement setup for measuring the edges of your choice, specifying trigger delays and measurement duration, and pacing measurements
- Sequential displays for characterizing PLL dynamics, viewing spindle speed variations, or verifying correctly written data patterns
- Computed clock for measuring to an ideal reference
- Timing pattern analysis for studying worst-case data patterns or viewing problematic data patterns and the surrounding code spacings
- Online Help for quick answers to operation questions
- Data export capability for transferring results to another analysis package or to spreadsheet or wordprocessor packages.

### Tributary Jitter Analysis

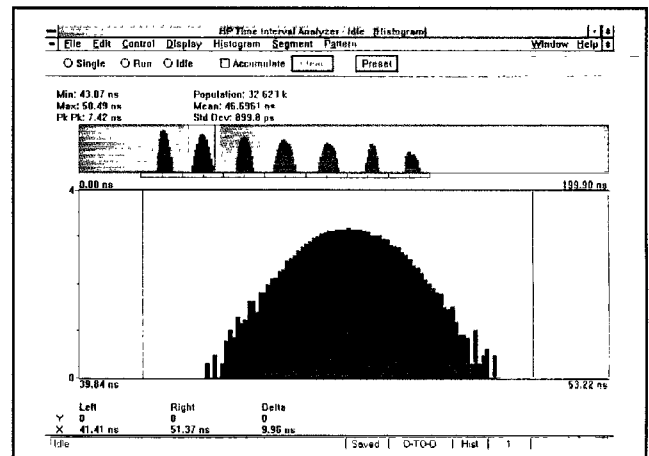
When integrating new SONET/SDH technologies with existing telecommunications equipment, network equipment designers use the HP E1725A TIA Option 242 tributary jitter analyzer software to make sure that new designs conform to evolving standards. HP's unique software clock extraction scheme and software filters provide consistent, repeatable results when measuring jitter. The display screens make it easy to examine mapping jitter, pointer-induced jitter, and waiting time jitter.

After a measurement is performed, the HP E1742A software (included in Option 242) extracts the clock signal and performs a variety of analysis functions:

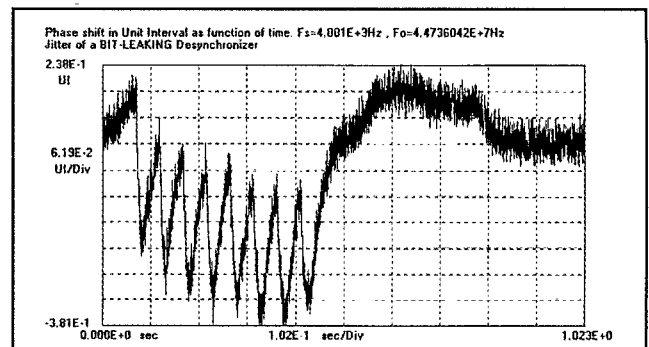
- Phase deviation display shows the cumulative phase difference of a signal relative to the extracted clock.
- Jitter display uses a built-in 10 Hz high pass filter to simultaneously display peak-to-peak jitter, positive peak, negative peak, mapping jitter, and other jitter components.
- Power spectrum display shows the frequency components which contribute to the jitter and gives a better understanding of the jitter sources.
- Frequency deviation display explains the effect of a pointer hit on the desynchronizer phase lock loop inside a network element.
- Allan variance, TVAR, and FFT functions enhance further study and analysis of the tributary jitter. Each measurement can be stored for future analysis. Graphic and numeric results can be transferred to other Windows applications for inclusion in documents or spreadsheets.



Settling time is displayed automatically on this direct measurement of the synthesizer step.



The HP E1741A features extensive statistical, histogram, and window margin analysis features to simplify jitter characterization in data storage products.



This HP E1742A display shows the peak-to-peak jitter during an 8 UI phase transient. The phase transient is being leaked out to the tributary over .5 seconds one bit at a time.